ALLOWANCE

1. Claims 1-15, 20-34, 36-37 are allowed.

Response to Arguments

2. In response to Applicant's remarks on page 9, the 35 U.S.C. 112, 2nd rejection is withdrawn. As such, claim 1 is interpreted to read that sets of input assignments are determined for each of a plurality of portions of the user design, and subsequently, all sets of input assignments are ranked (Specification, [0039]).

3. Regarding Applicant's remarks on pages 10-12, as well as the interview summary, a set of input assignment consists of a signal assigned to an input port of fixed-configuration secondary hardware (Specification, [0040]-[0041], Figure 5 Example Set of Input Assignments).

REASONS FOR ALLOWANCE

4. The following is an examiner's statement of reasons for allowance:

Applicants are disclose a method and medium for using a computer system to determine an implementation of a user design on a programmable device including a plurality of programmable logic elements, each comprising reconfigurable logic hardware and fixed-configuration secondary hardware, wherein the fixed-configuration secondary hardware has a plurality of inputs, the inputs common to at least two of the programmable logic elements, the method comprising: for each of a plurality of portions of the user design, determining, with at least one processor of the computer system one or more sets of input assignments of signals in the user design to the fixed-configuration secondary hardware, each set providing an implementation of a logic function of that portion of the user design using the fixed-configuration secondary hardware. This has been disclosed in the prior art of record.

The prior art of record does not disclose the method and medium wherein *ranking, with the processor, the sets of input assignments by determining a number of times each set is assigned to the*

fixed-configuration secondary hardware; and selecting, with the processor, a highest ranked set of input assignments, wherein the highest ranked set is assigned to the fixed-configuration secondary hardware at least two or more times; and creating, with the processor, an implementation of a subset of the portions of the user design by implementing the selected set of input assignments as inputs to a corresponding subset of the plurality of fixed-configuration secondary hardware.

The closest prior art uncovered during examination teaches certain limitations of the claimed invention as follows:

U.S. Patent No. 6,195,788 B1, Leaver et al.: Discloses ranking, with the processor, the sets of input assignments **(column 10, lines 1-15, Table 1)**; and selecting, with the processor, a highest ranked set of input assignments **(column 10, lines 41-64)** and creating, with the processor, an implementation of a subset of the portions of the user design by implementing the selected set of input assignments as inputs to a corresponding subset of the plurality of fixed-configuration secondary hardware **(column 7, lines 52-64)**. However, Leaver fails to disclose wherein the ranking, with the processor, the sets of input assignments by determining a number of times each set is assigned to the fixed-configuration secondary hardware, wherein the selecting the highest ranked input assignment is assigned to the fixed-configuration secondary hardware at least two or more times.

U.S. Patent No. 6,526,557, Young et al.: Discloses ranking and selecting frames for configuration data for memory cells **(column 9, lines 19-29)**. However Young fails to disclose wherein the ranking, with the processor, the sets of input assignments by determining a number of times each set is assigned to the fixed-configuration secondary hardware, wherein the selecting the highest ranked input assignment is assigned to the fixed-configuration secondary hardware at least two or more times.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. U.S. Patent No. 5,748,488 issued to Gregory et al. on 05/05/98.
2. U.S. Patent No. 6,086,626 issued to Jain et al. on 07/11/00.
3. U.S. Patent No. 6,026,230 issued to Lin et al. on 02/15/00.
4. U.S. Patent No. 7,020,864 B1 issued to Loong on 03/28/06.
5. U.S. Patent No. 6,990,650 B2 issued to Teig et al. on 01/24/06.
6. "BDD-Based Logic Synthesis for LUT-Based FPGAs" published by Vemuri et al. in 10/2002.
7. "Performance evaluation and optimal design for FPGA-based digit-serial DSP functions" published by Lee et al. on 11/15/02.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUZANNE LO whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128

/SL/
08/11/09